ELL304

Experiment-2 Report

Single Device Amplifiers

Table 23 (Monday)

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# Aim

To characterize single-MOSFET amplifiers.

1. Resistive biasing
2. Common source amplifier
3. Common gate amplifier
4. Common drain amplifier

# Apparatus Required

* CD4007 IC
* Breadboard
* Oscilloscope
* DC Source Generator
* Function Generator
* Resistances
* Capacitors

# Theory

* With proper biasing, the MOSFET will provide amplification for small signal inputs.
* We are only interested in the saturation region of the MOSFET operation. That is, we need to bias our MOSFET such that *VDS > VGS* − *VTh* for an nMOS.
* Our baising is such that we are providing *VG* via a resistive divider. The value of

*VG* is given as: .

* The value of *VD* is given as: *VD* = *VDD* − *IDRD*.
* The value of *VS* is given as: *VS* = *IDRS*.
* Since we an directly measure all the above three voltages, we can also calculate *ID* using any of the previous two relations.
* **Common Source Amplifier:** In a common source amplifier, input is connected at the gate and output is taken at the drain of the MOSFET. A common source amplifier

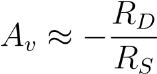
is an inverting amplifier where the output is phase shifted by 180◦. The gain obtained is given as:

resistance at drain *gmRD*

*Av* = − = −

resistance at source 1 + *gmRS*

Since *gmRS* ≫ 1,



* **Common Gate Amplifier:** In a common gate amplifier, input is connected at the source and output is taken at the drain of the MOSFET. A common gate amplifier is a non-inverting amplifier. It is also known as a current buffer since the input and output current is same. The voltage gain obtained is given as:

*Av* = *gmRD*

* **Common Drain Amplifier:** In a common drain amplifier, input is connected at the gate and output is taken at the source of the MOSFET. A common drain amplifier is also known as a voltage buffer, since the input and output voltage is same. Thus, the gain obtained here is theoretically:

*Av* ≈ 1

# Resistive Biasing

## Procedure

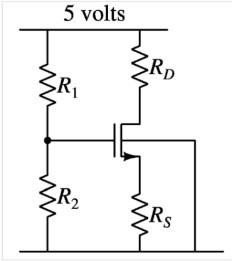


Figure 1: Circuit Diagram for part 1

* Circuit was connected as shown in circuit diagram.
* The value of resistors used was: *Rs***=10k**Ω**,** *RG*1**=100k**Ω **and** *RG*2**=330k**Ω.
* Gate-source and drain-source voltage readings were taken for different values of *RD* varying from 33kΩ to 0.

## Readings

*VDD* = 5 V

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *RD* (Ω) | *VG* (V) | *VD* (V) | *VS* (V) | *ID*(mA) | *VDS*(V) | *VGS* (V) |
| 33000 | 3.76 | 1.49 | 1.35 | 0.135 | 0.14 | 2.41 |
| 10000 | 3.76 | 2.68 | 2.28 | 0.228 | 0.4 | 1.48 |
| 3300 | 3.76 | 4.16 | 2.32 | 0.232 | 1.84 | 1.44 |
| 1000 | 3.76 | 4.72 | 2.36 | 0.236 | 2.36 | 1.4 |
| 470 | 3.76 | 4.84 | 2.36 | 0.236 | 2.48 | 1.4 |
| 100 | 3.76 | 4.92 | 2.36 | 0.236 | 2.56 | 1.4 |
| 0 | 3.76 | 5 | 2.36 | 0.236 | 2.64 | 1.4 |

Table 1: Measurements of *VGS* and *VDS* and calculation of corresponding *ID*

## Circuit Snapshot

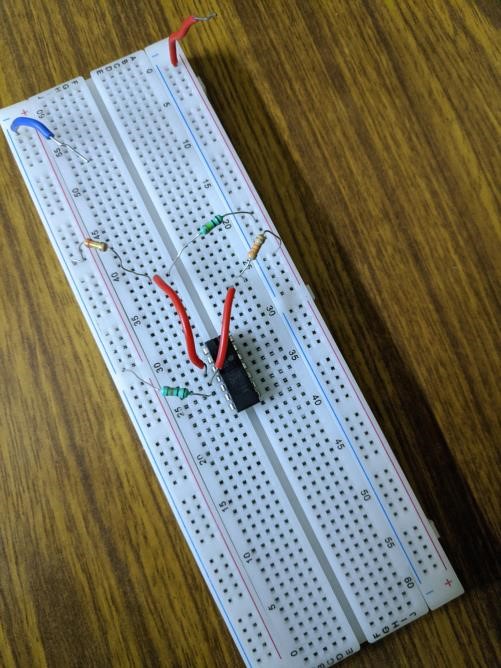


Figure 2: Connections snapshot for Part 1

## Graphs

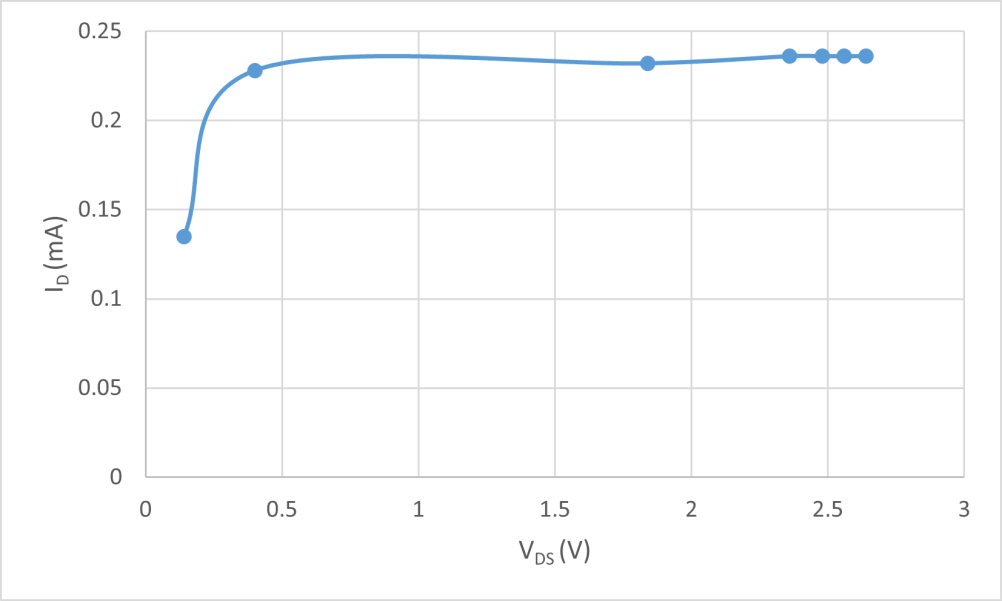


Figure 3: *ID* vs *VDS*

## Observations

* We get some current with *RD*=33kΩ. On decreasing this resistance *RD* (thus increasing *VDS*), the current increases.
* Below a certain *RD*, the current saturates.
* The current was very low at *RD*=33kΩ.
* When we make *RD*=10kΩ, the current increases.
* When we make *RD*=0 (short), the current is almost same as with *RD*=10kΩ.
* The largest (available) *RD* for which the current does not change is found to be 10kΩ.

# Common Source Amplifier

## Procedure

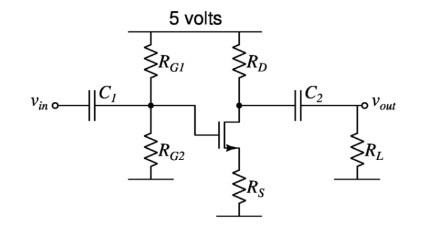


Figure 4: Circuit Diagram for common source amplifier.

*RD* = 10kΩ, *RS* = 10kΩ, *RG*1 = 330kΩ, *RG*2 = 100kΩ, *RL* = 100kΩ, *C*1 = *C*2 = 22*µ*F

* Connections were made as shown in circuit diagram.
* The resistance values used were *RD*=10kΩ, *RS*=10kΩ, *RG*1=330kΩ, *RG*2=100kΩ and *RL*=100kΩ. The capacitance used were all 22 *µ*F.
* A 100mV pk-pk 100Hz sine wave was injected at *vin*. And voltage gain was measured from *vout/vin*. • Source frequency was increased till 1MHz and the above measurement was repeated each time.

## Readings

**DC operating point**: *VG* = 3.76V, *VD* = 3.54V, *VS* = 1.72V

Therefore, *VDS* = 1.82V and *VGS* − *VTh* = 2.04V-0.9V = 1.14V. Hence, *VDS > VGS* −*VTh*.

**Small signal readings**: *vin* = 106mV pk-pk sine, *VDD* = 5 V

|  |  |  |
| --- | --- | --- |
| Frequency (Hz) | *vout* (mV) | |Gain| = |*vout/vin*| |
| 100 | 58 | 0.54 |
| 3000 | 52 | 0.49 |
| 4000 | 52 | 0.49 |
| 5000 | 52 | 0.49 |
| 10000 | 45 | 0.68 |
| 20000 | 39 | 0.368 |
| 30000 | 30 | 0.283 |
| 40000 | 26 | 0.245 |
| 50000 | 25 | 0.235 |
| 60000 | 23 | 0.217 |
| 100000 | 20 | 0.189 |
| 1000000 | 17 | 0.16 |

Table 2: Measurements of *vout* and calculation of corresponding gain for Common Gate Amplifier

## Circuit Snapshot

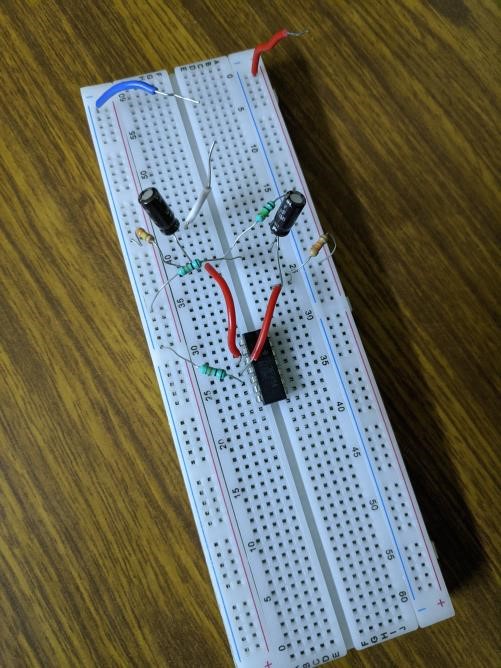


Figure 6: Connections snapshot for Part 2

## Graphs

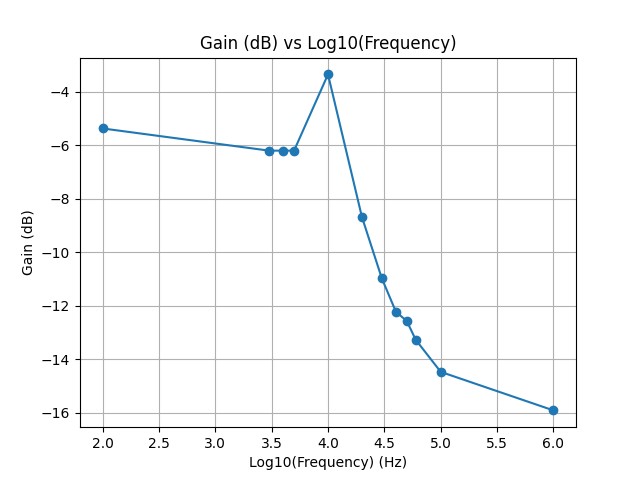


Figure 7: Gain (dB) vs *log*10(frequency) plot

## Observations

* We observe that we get a small signal gain of around ~ 0.54
* Initially, the gain is almost unchanging on changing frequency.
* We also observe that after around 400kHz, on increasing frequency, the gain decreases drastically.

# Common Gate Amplifier

## Procedure

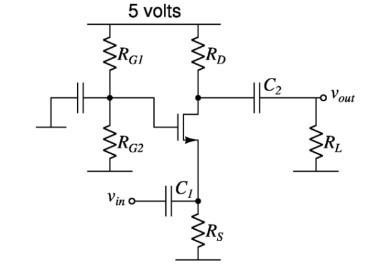


Figure 8: Circuit Diagram for common gate amplifier.

*RD* = 10kΩ, *RS* = 10kΩ, *RG*1 = 330kΩ, *RG*2 = 100kΩ, *RL* = 100kΩ, *C*1 = *C*2 = 22*µ*F

* Connections were made as shown in circuit diagram.
* The resistance values used were *RD***=10k**Ω**,** *RS***=10k**Ω**,** *RG*1**=330k**Ω**,** *RG*2**=100k**Ω **and** *RL***=100k**Ω. The capacitance used were all **22** *µ***F**.
* A 100mV pk-pk 100Hz sine wave was injected at *vin*. And voltage gain was measured from *vout/vin*. • Source frequency was increased till 1MHz and the above measurement was repeated each time.

## Readings

**DC operating point**: *VG* = 3.76V, *VD* = 3.31V, *VS* = 1.72V

Therefore, *VDS* = 1.59V and *VGS* − *VTh* = 2.04V-0.9V = 1.14V. Hence, *VDS > VGS* −*VTh*.

**Small signal readings**: *vin* = 90mV pk-pk sine, *VDD* = 5 V

|  |  |  |
| --- | --- | --- |
| Frequency (Hz) | *vout* (mV) | |Gain| = |*vout/vin*| |
| 100 | 368 | 4.09 |
| 500 | 360 | 4.00 |
| 1000 | 360 | 4.00 |
| 5000 | 360 | 4.00 |
| 10000 | 360 | 4.00 |
| 50000 | 300 | 3.33 |
| 100000 | 225 | 2.50 |
| 500000 | 54 | 0.60 |
| 1000000 | 30 | 0.33 |
| 2000000 | 15 | 0.17 |
| 3000000 | 15 | 0.17 |
| 4000000 | 14 | 0.16 |

Table 3: Measurements of *vout* and calculation of corresponding gain for Common Gate Amplifier

## Circuit Snapshot

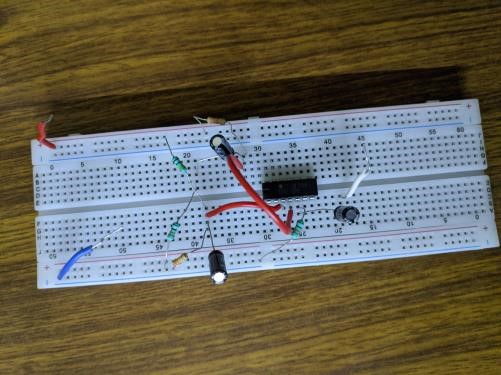


Figure 10: Connections snapshot for Part 3

## Graphs

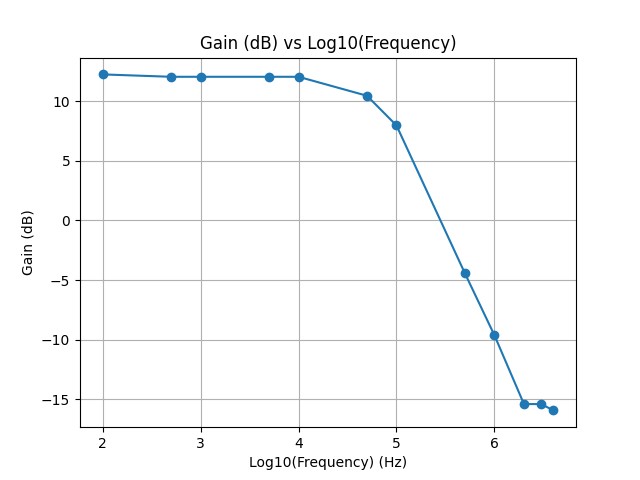


Figure 11: Gain (dB) vs *log*10(frequency) plot

## Observations

* We observe that we get a small signal gain of ˜4.09.
* Just like common source, here also the gain drops close to zero at very high frequencies. Here, above 600kHz, there is a significant drop in gain.

# Common Drain Amplifier

## Procedure

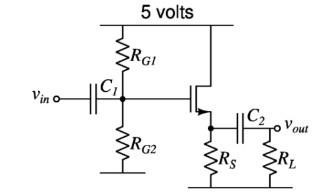


Figure 12: Circuit Diagram for common drain amplifier.

*RS* = 10kΩ, *RG*1 = 330kΩ, *RG*2 = 100kΩ, *RL* = 100kΩ, *C*1 = *C*2 = 22*µ*F

* Connections were made as shown in circuit diagram.
* The resistance values used were *RS*=10kΩ, *RG*1=330kΩ, *RG*2=100kΩ and *RL*=100kΩ. The capacitance used were all 22 *µ*F.
* A 100mV pk-pk 100Hz sine wave was injected at *vin*. And voltage gain was measured from *vout/vin*. • Source frequency was increased till 1MHz and the above measurement was repeated each time.

## Readings

**DC operating point** : *VG* = 3.76V, *VD* = 5V, *VS* = 1.82V

Therefore, *VDS* = 3.18V and *VGS* − *VTh* = 1.94V-0.9V = 1.04V. Hence, *VDS > VGS* − *VTh*.

**Small signal readings** : *vin* = 90mV pk-pk sine, *VDD* = 5 V

|  |  |  |
| --- | --- | --- |
| Frequency  (Hz) | *vout* (mV) | |Gain| = |*vout/vin*| |
| 100 | 74 | 0.82 |
| 500 | 74 | 0.82 |
| 1000 | 74 | 0.82 |
| 5000 | 74 | 0.82 |
| 10000 | 74 | 0.82 |
| 50000 | 74 | 0.82 |
| 100000 | 73 | 0.81 |
| 500000 | 68 | 0.76 |
| 1000000 | 54 | 0.60 |
| 2000000 | 36 | 0.40 |
| 3000000 | 28 | 0.31 |
| 4000000 | 26 | 0.29 |

Table 4: Measurements of *vout* and calculation of corresponding gain for Common Drain Amplifier

## Circuit Snapshot

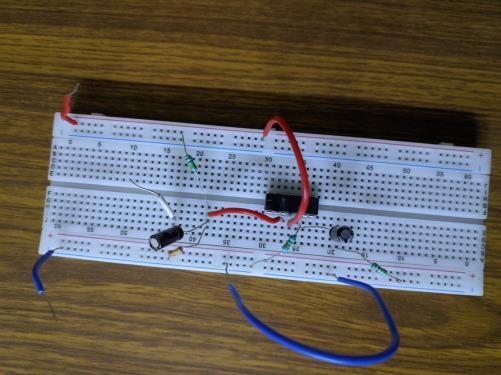


Figure 14: Connections snapshot for Part 4

## Graphs

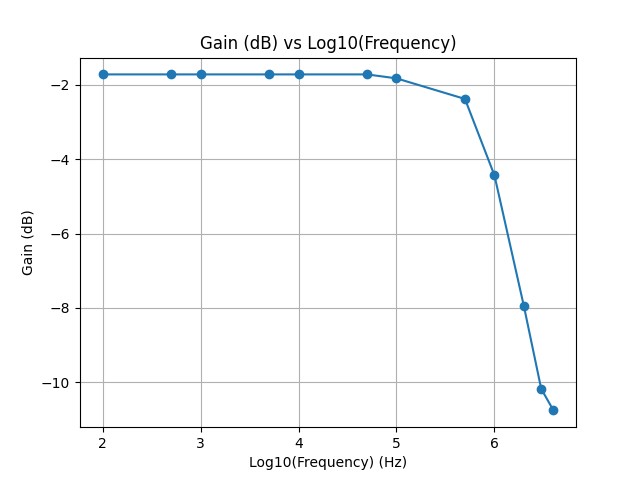


Figure 15: Gain (dB) vs *log*10(frequency) plot

## Observations

* We get a small signal gain of ˜0.82.
* Again, the gain drops significantly at higher frequencies after 500kHz.

# Conclusion

* **Resistive Biasing**: When the drain voltage is above overdrive voltage in an nMOS,

i.e., when the nMOS is in saturation, the device current remains constant.

* **Common Source Amplifier**: The gain obtained is ˜ 0.68, which is the expected gain from theory. Since we are using *RD* = *RS* = 10kΩ, the approximate gain is around 1. If we calculate the exact value without approximation using  and using

 , we get a value smaller than 1 (around 80%). Due to practical

limitations, we do not get an exact gain, and hence within the practical bounds, our observations match with theory.

* **Common Gate Amplifier**: The gain obtained is ˜4.09, which is the expected gain from theory within practical bounds. Also, the gain decreases by 3dB at around 100kHz
* **Common Drain Amplifier**: The gain obtained is ˜0.82 which is very close to the source follower property of common drain amplifier. Within practical bounds, the theoretical value matches the experimental value. Also, the gain decreases by 3dB at around 1MHz.
* We observed that the gain in all the three configurations is nearly constant in lower frequencies and then suddenly drops considerably when frequency is increased. We can see this in the graphs plotted which resemble a low pass filter. This can be explained by the parasitics. At higher frequencies, the parasitic capacitances start to show their effect. The impedances of parasitic capacitance of the MOSFET become comparable to the biasing impedances in the circuit. Hence, all the current now does not flow through the load resistors and hence the output voltage also decreases.

